Dynamic Behavior Model for SEED Analysis; Extraction using Surface Response Modelling

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Dynamic Behavior Model for SEED Analysis; Extraction using Surface Response Modelling

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Abstract - **System Efficient ESD Design (SEED) requires dynamic behavior models from the devices and circuitry used along the protection chain, typically from the discharge point of entry at the PCB boundary i.e. connector up to the circuits on-chip to be protected. In-between this path there may be external ESD protection i.e. voltage clamping together with parasitic layout effects, interconnect path delay with specific transmission line properties, package design up to on-chip protection design with parasitic layout effects and ultimately the on-chip circuit(s) to be protected, being unpowered or powered.**

By using the full voltage/current versus time-domain response of an ESD protection device with the TLP test method [3 - 5], while knowing the excitation profile as generated by the TLP system, a high-order equivalent model can be extracted from the data.

In this paper a proposal for a DoE multi-parameter statistical behavior model will be given together with the rationales [1, 2].

Keywords — System efficient ESD design (SEED), transmission line pulse (TLP), time- frequency-domain, dynamic behavior model

I. Introduction

Per today, the ESD protection devices are represented by their response parameters obtained from a TLP test after 70% of the pulse duration [3 - 5]. Whatever response has happened at the beginning of the pulse is ignored, while it is the most critical part of the response when one wants to protect high-speed devices.

Today's TLP systems (e.g. HPPI [6], EMCESD [7]) have an extended measurement bandwidth of more than 2 GHz, while using signal sampling rates of 10 GS/s or more. As such, device response data can be obtained from 100 ps to the full span of 100 ns (typical pulse duration), see figure 1. This bandwidth extension also requires an adaption of the voltage and current measurements to ensure correct data (after de-embedding).

Various analog circuit simulation methods (SPICE) can be used to apply the response data while using a look-up table which is quite cumbersome. More suited compact behavior models are needed which can be used in either time or frequency domain. Following SPICE syntax, voltage, current, time delay, time and its derivatives can be used to develop a time-domain behavior model. Unfortunately, this time-domain based behavior model then cannot be used with frequency domain analysis.

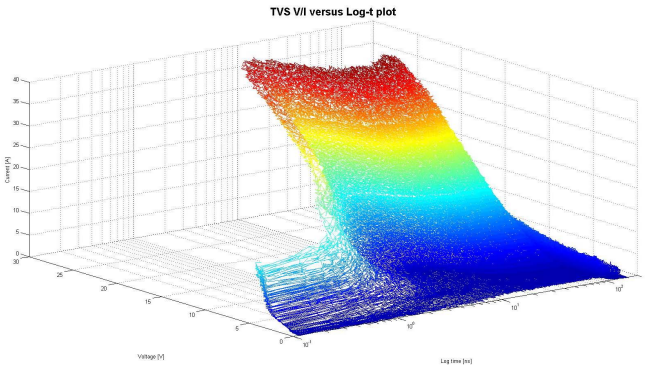

Figure 1 - I/V versus log-time response

With the behavior model approach chosen, a surface fitting response analysis is chosen following a design of experiments (DoE) statistical approach using the Box-Bencken technique [1, 2]. For the sake of deriving a proper model with an initial response in the sub-nanosecond region, the time scale is converted to a log-scale rather than using it as a linear variable. Voltage, current (or impedance) can be converted too into the logarithmic domain, in particular when one wants to analyze the transient response from the functional domain, assuming nA to µA leakage current versus the tens of amps during the TLP event. Even so, the voltage will vary from a few volts functional to about 100 volts during the TLP initiated trigger and clamping conditions.

It is the aim of this project to set up a fully automated parameter extraction sequence, using this DoE statistical method, by which the TLP obtained measurement data can be converted to a behavior model suited in a SPICE simulation environment with a minimum amount of measurement runs.

II. Problem Analysis

Common, when a spice model is derived for transient suppressors: arrestors, varistors, TVS-diodes, often controlled voltage and current sources are used within the model while

the device is passive and cannot generate any energy itself. Another approach would be to use the physical elements of the design and put these into expressions to represent the behavior of the device or circuit in certain regions, like is done with semiconductor devices e.g. BSIM3. Using simple spice elements in combination with lookup tables as with IBIS modelling is another approach.

On the other hand, the computational effort has to be kept low as the device response is needed over a wide time range; 1/10 of a nanosecond to hundreds of nanoseconds (factor 1000) and I/V values ranging from volts to kilovolts (factor 1000) and micro- or nano-amps to tens of Amps (factor 10^6 - 10^9). Due to the large ranges in the linear scale domain it is an advantage to transfer those values to a more compact range on a log-scale.

Yet another challenge occurs w.r.t. the data capturing as the vertical resolution from high-speed oscilloscopes is limited to 8 bits typical (• factor 256). When taking measurements in the time domain, oversampling doesn't help to enhance the vertical resolution for a single occurrence. Taking multiple sequential measurements, with or without a slight delay in triggering will not work either unless device heating is ignored and these multiple measurements are considered independent and assumed periodic. Taking multiple measurements with a known trigger delay will only help to enhance the reliability of the data in the sub-nanosecond region (horizontal resolution), when properly mapped.

To obtain sufficient information, to be used to derive a surface response, steps need to be taken in de voltage domain e.g. 5/decade (1, 2, 3, 5, 8, 10) or a decimated version with only 2 steps (1, 3, 10) or just 1 step per decade. These options provide a near linear step in the log amplitude-domain.

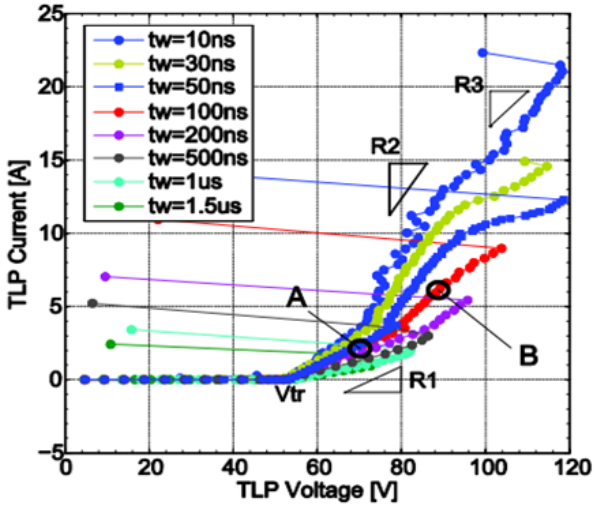

Figure 2 - 70% pulse responses as function of pulse length

Each device or circuit to be modelled has an intrinsic inductance, determined by the electrical path length through the device, leading to: $U_L = L.di/dt$. Furthermore, the device or circuit has an intrinsic capacitance which affects the response too: $I_C = C.dU/dt$. The dynamic resistance is determined by the voltage applied and may have a snap-back behavior. This snap-back is heavily determined by the rise time of the pulse applied and the pulse duration i.e. at which moment in time the 70% values for voltage and current are taken in relation to the self-heating of the device. With static DC voltage increments, e.g. using an SMU, snap-back effects don't occur. At last, devices/circuits will show a delay in their startup, which is partly caused by the delay of the intrinsic LC-elements (self-resonance) of the device/circuit used and/or partly needed by the charge necessary to start or to get triggered.

III. Statistical Analysis

When using a DoE statistical analysis approach, one has to define the number of input parameters and the ranges i.e. levels which will be taken for each parameter, commonly x ± •x, see figure 3. The input parameters considered are: TLP charge voltage (3 levels: low, mean, max.), rise time (3 levels: very fast, fast, dull), pulse duration (3 levels: 10, 100, 1000 ns), polarity (2 levels: pos./neg.), impedance (2 levels: 50 and 500 •). The combination of the 2- and 3-level parameters results in a total run of only 54 combinations. An extra impedance level like Human metal model (HMM) with TLP makes no sense as it is NOT an impedance on a progressive scale. If polarity and impedance are excluded from the experimental setup, only 15 runs result. Even less runs result when a Taguchi statistical analysis method is chosen instead of Box-Bencken. This Taguchi analysis is solely useful when all parameters are non-confound. Full-factorial analysis results in 162 experimental runs.

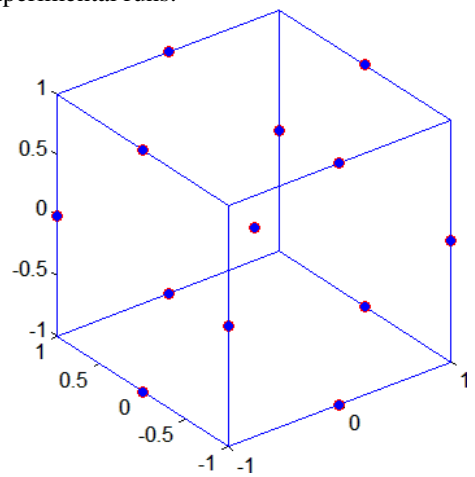

Figure 3 - Box-Bencken 3 x 3 experimental space

Secondly, one has to define the responses (vectors rather than single scalars which are needed for further reduction criteria) towards which a correlation needs to be found. Here a number of parameters are considered: response delay: time

necessary to reach the clamping voltage, trigger voltage: a minimum voltage necessary to trigger the device and often related to the rise time, dV/dt: for edge triggered devices, clamp voltage, dynamic impedance, snap-back behavior, oscillations, self-heating (with long pulses or high(er) pulse repetition rates, see figure 2), charge recovery (storage effects), etc. What shall be considered too are the intrinsic inductances of the device or circuit and the intrinsic capacitance. The latter may be affected by DC-biasing when depletion capacitances are considered. When these intrinsic parameters are known, these can be used with further analysis. Otherwise these shall be used as input parameters. Outside the scope of this analysis are the die or PCB routing parameters which will affect the responses too.

From the few I/V versus time responses, as defined by the statistical analysis method used, all these response parameters can be drawn. Additionally, also the I/V time derivative and the I/V time integral can be taken to obtain further information and better insight in the intrinsic capacitance and inductance of the device or circuit. In particular, the derivative is chosen to determine the delay between the V- and I- versus time responses. Again a criterion needs to be set w.r.t. the threshold level at which the delay is specified.

IV. Calibration

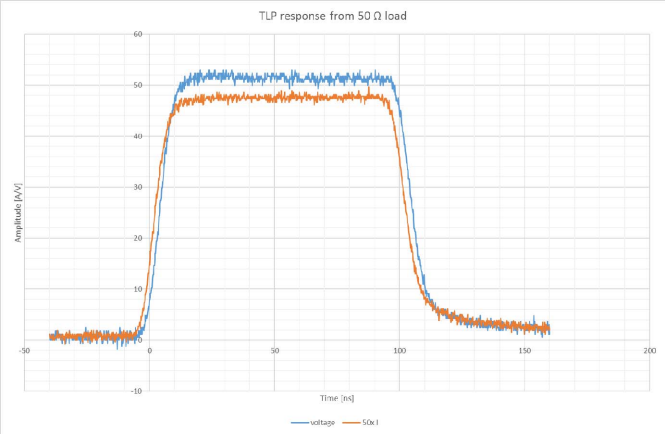

Figure 4 – Uncorrected pulse responses of a 50 • resistor

Before device or circuit measurements are taken, the TLP test setup needs to be calibrated, de-skewed and possibly de-embedded, this to ensure the correctness of the data obtained. W.r.t. the input parameters to be set, these have to stem with the 2- or 3-level values as used with the analysis model for which the voltage levels: low, mean, max. have to be chosen within the range that the device or circuit can handle. For the charge voltage polarization, this is clear as only 2 levels apply. For impedance, the exact value needs to be obtained, similar as for the charge voltage, the rise time and the pulse duration. As indicated earlier, the intrinsic inductance as well as the intrinsic capacitance of the whole setup play an important role w.r.t. the impedance reference plane defined as the test setup will change the values found by the PCB layout used. Using an SMD resistor for calibration may look nice after 70% of the pulse duration but may yield a significant inductance, thus resulting in overshoot, while measuring in the sub-nanosecond range. If such an SMD resistor is used as reference with a TLP response calibration, the length of the current path, being the physical length of the resistor, is nullified and will no longer show up.

The way of measurement, using voltage and current probes at the DUT end or in the cables or using directional couplers: measuring forward and reflected power or other means of response measurement affects the results too. With separate current and voltage probes the exact location of the two probes need to be corrected for but often the frequency dependency or even worse the amplitude dependency (saturation effects) will be critical and need thorough corrections afterwards. The current probe has physical length and causes stray inductance and the broadband voltage probe represents some load. Measuring the voltage before or after the current probe makes significant difference unless calibrated and corrected for.

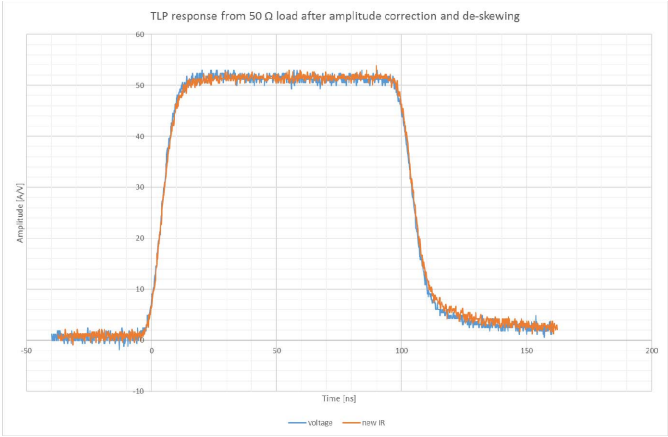

Figure 5 – Corrected pulse responses of a 50 • resistor

Current/voltage de-skewing can be done by using an ideal short, open and load, in a similar manner like the calibration of a RF vector network analyzer (VNA). In case of a matched line: 50 • in case of the TLP, no reflections are expected and the voltage and current wave shapes should fully coincide. In figure 4 an example is given where after a formal TLP test system calibration (according the supplier) still a skew and an amplitude error results, non-causal as the current comes before the voltage is there. The corrected results are given in figure 5. A time error of 2,4 ns needs to be corrected and an amplitude correction of more than 8% to fit the lines closely.

However, when more focus is put on the initial behavior of the pulse, one can see that there is still a slight mismatch. Furthermore, much more detail can be found on a log-time scale, see figure 6. When there is no transient voltage, no current will result through the 50 • resistor too and no

impedance can be derived. In this particular case, considering an 0603 shape SMD and a TLP (charge) voltage applied being 100 volts, 50 volts should result at t = 0^+, extended by the L.di/dt of the component.

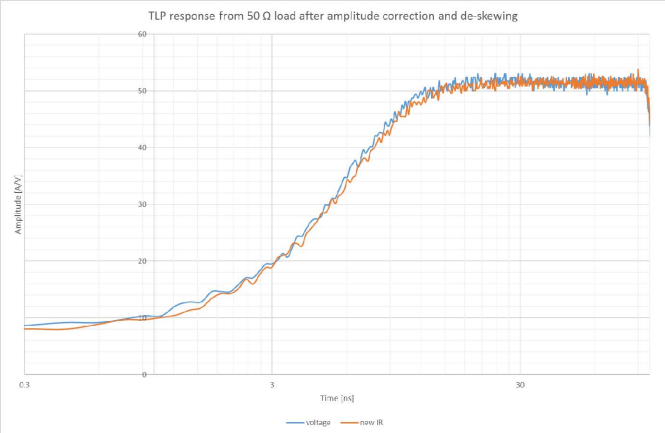

Figure 6 – Corrected pulse responses on a log-time scale

The inductance is proportional to the path length though the SMD resistor, from solder pad upwards to the top metal film layer and then backwards to the solder pad. The current path meets twice the physical height of the component (unless mounted face down), plus the metal film length, assuming a homogeneous resistance without laser trimming adjustments. If 1,6 mm, see figure 7, is taken as a path length and the rise time of the TLP is 600 ps, the current will grow at 1,66 A/ns. A small voltage hump of more than 2 volts is expected at the start of the voltage wave shape i.e. a small delay of the current. As a result of the inductive part in series, the impedance versus time should start higher than the mean value at 70% of the pulse duration, being 49,7 •, rather than 53,8 • as obtained from the raw data.

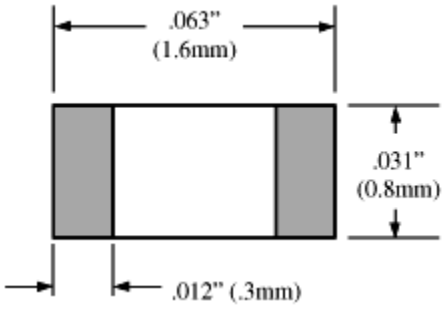

Figure 7 - 0603 SMD footprint

As stated before, the electrical path length (= inductance) has been nullified during calibration and will not show up any further, see figure 8. What can be seen too is that the current probe has limited bandwidth on the low side due to the impedance increase at the end of the pulse (~100 ns).

Performing a correct calibration, combined with de-skewing and de-embedding is essential before the statistical data obtained can be used for further analysis of a device or circuit model extraction. This is particular important when the sub-nanosecond region needs to be analyzed too rather than only after 70 ± 5 or 10 % of the pulse duration.

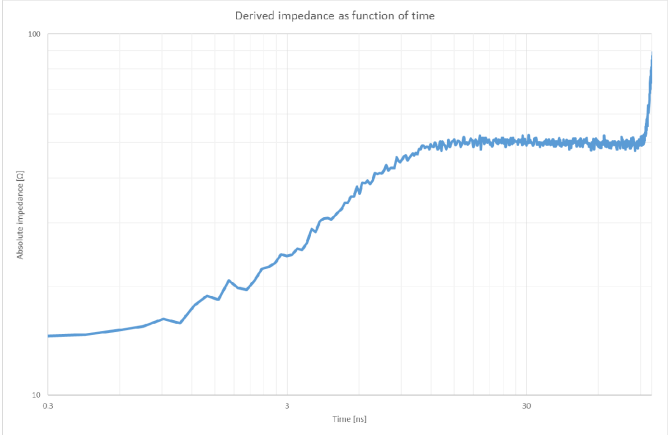

Figure 8 – I/V ratio versus time (after calibration)

V. Surface Model Extraction

A surface response function can be drawn from the raw data measured but appears little useful considering the errors as indicated above. Based on the data available a first attempt will be presented at the symposium. Application notes [8, 9] indicate that industry struggles with the use and the usefulness of the TLP test methods as presently defined. Modelling the static responses

VI. Conclusion

The statistical analysis method (Box – Bencken) proposed still needs to prove its validity. For this, the correct measurement data as defined by the exploration matrix is inevitable. The dynamic behavior model for SEED analysis is possible when the rules are obeyed and the input combination parameters are correctly taken. The device model can be extracted using surface response modelling. Modelling the near static responses at 70% while living in a USB-3C environment of 10 Gb/s becomes a waste of effort.

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