Resonant-Free PDN Design®

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Resonant Free PDN Design

Presentation outline

- Introduction
- Overview
- New approach
- Conclusions

Introduction

- With nanometre scaling, the amount of transistors/chip will follow Moore's Law.
- On- and off-chip clock and data speeds will increase further.
- Core supply voltages are reduced further down to below 1 Volt
- Peripheral supply voltages have to follow international agreed voltages levels to enable interfacing.

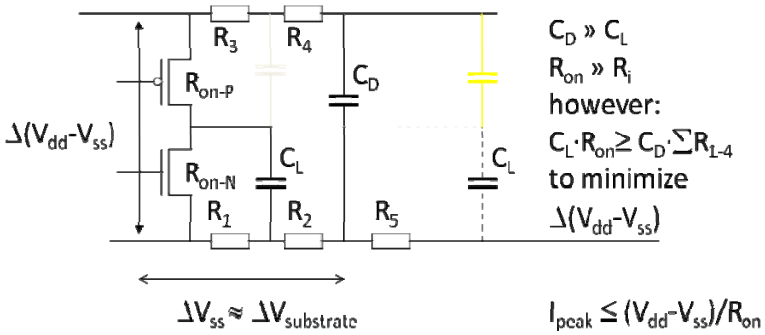
Introduction

- While lowering the core supply voltages, the on-chip noise margin will drop accordingly
- Tight on- and off-chip decoupling measures are necessary.
- Typically, RF switching noise from digital designs are forced out of their packages through the supply and ground pins when applying conventional off-chip decoupling

Overview of measures

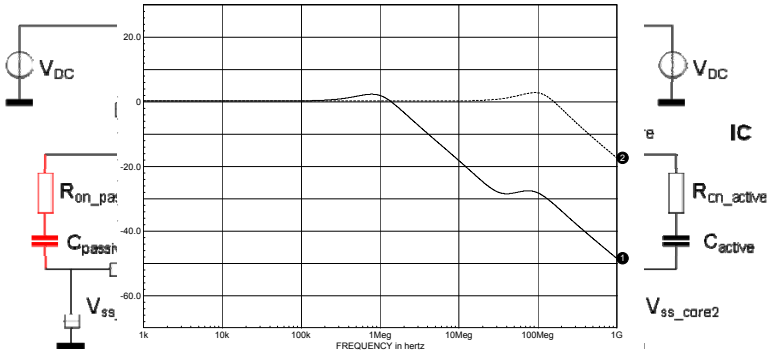
- On-chip measures
  - On-chip decoupling; needed for operation
  - Spread-spectrum; spreading in frequency domain
  - Multi-phase clocking; spreading in time domain
  - Embedded LDO; current confinement
  - Variable voltage, variable frequency
- Off-chip measures
  - Kelvin contacts
  - Complementary off-chip measures
  - Resonance free PDN design

Overview (of what has been done)



- **Supply bounce; IR-drop and delay**
- **V_{ss}-net/substrate analysis**

Overview (of what has been done)



Current confinement by Kelvin contacts for Off-chip decoupling

New approach

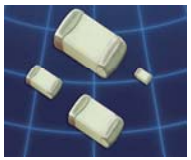
- On-chip decoupling is always present: µC, DSP, FPGA, etc. both for core and peripherals
- Equivalent package induction with <u>on-</u>chip capacitance is at resonance below 100 MHz: example: 200 nF + 0,2 nH → ~25 MHz
- When ideally decoupled <u>off-</u>chip quality factor of resonance > 10 is reached
- Need for dampening !! (in example just 31 mΩ **!!**)

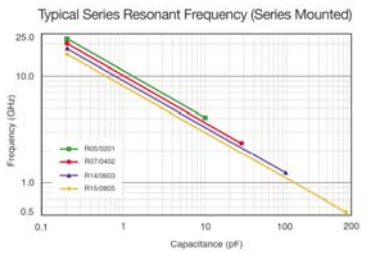
New approach

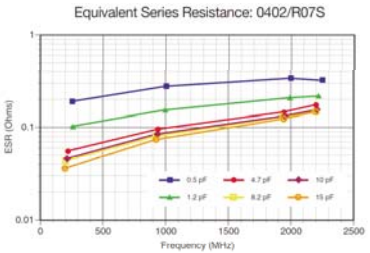
- Multiple decoupling capacitors are root cause for resonances. Values: 1:10:100:1000 are typ. placed in parallel to cover whole frequency range. ESL and physical distance add inductances thus resonances
- Multiple supply/ground planes in parallel in a multilayer PCB structure are additional root cause for resonances. Open and short-circuited TL-ends cause steep resonances from several MHz into GHz range

New appraoch

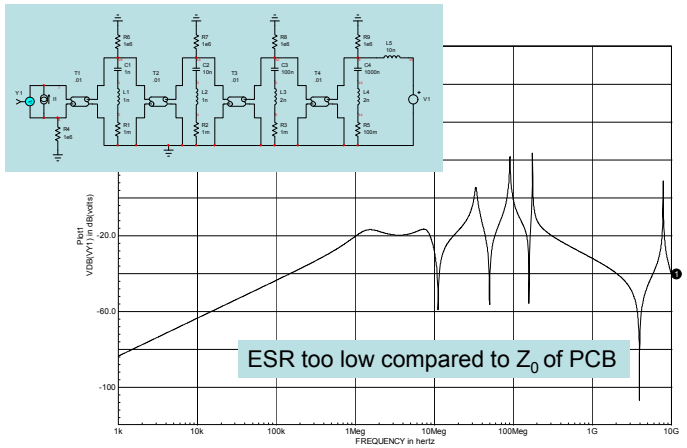
- Ceramic multilayer capacitors have resonance frequency in GHz range with Q > 1000, larger capacitance → lower ESR







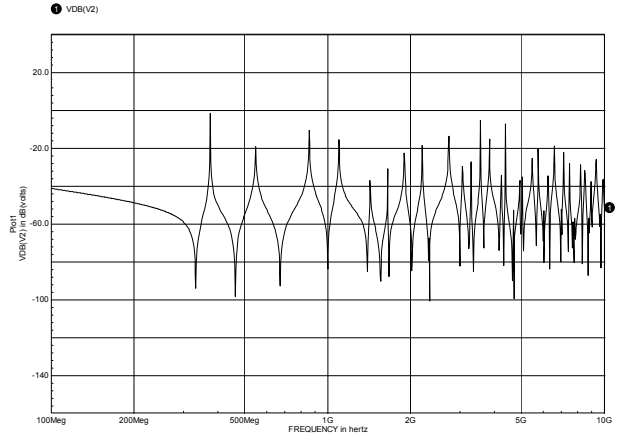
Multiple decaps in parallel



New approach

- Inter-plane characteristic impedance is between 0,1 and 2,5 Ω. Multiple plane pairs can be used in parallel
- Port impedance is $Z_0/4$ as signals are propagation to all 4 edges or when rotation symmetric diverging; $Z_0/2\pi$
- Port impedances less than 10 mΩ easy achievable; 3 plane pairs at 100 μm spacing

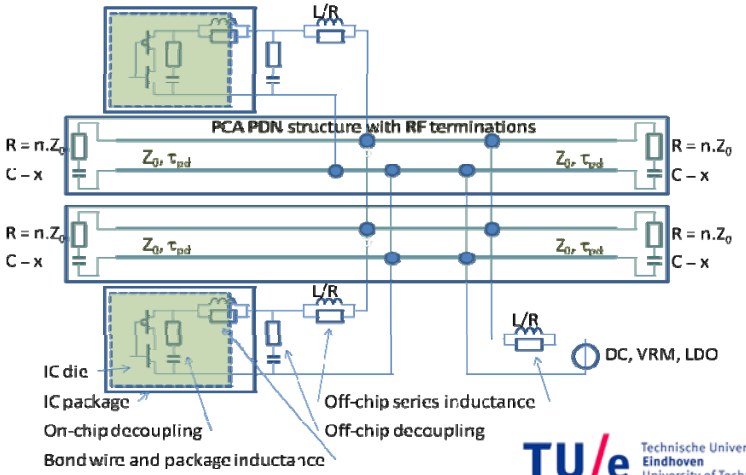
Off-center port on Euro-card, Z_0 = 10 mΩ



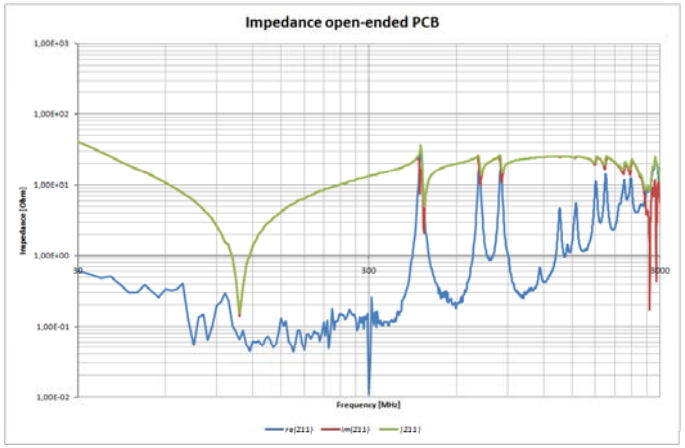
New approach

- The whole PDN chain from DC supply to the IC supply pads needs to be considered
- All “taps” and “feeds” shall:
  - impedance » $Z_0/4 \geq f_{crit.}$
  - resonant free; Q ≤ 2
- Due to skin and proximity effects full insulation between supply/ground currents and signal return paths are achieved
  skin depth = 6 μm @ 100 MHz, Cu-layer = 37 μm

Total Resonant-Free PDN solution



Device port impedance Z_{11}



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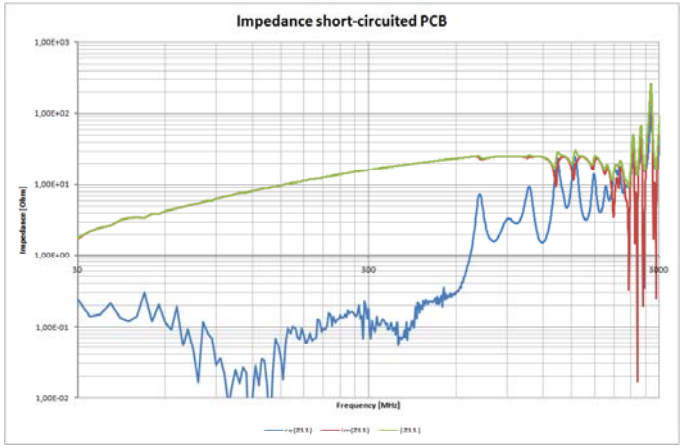

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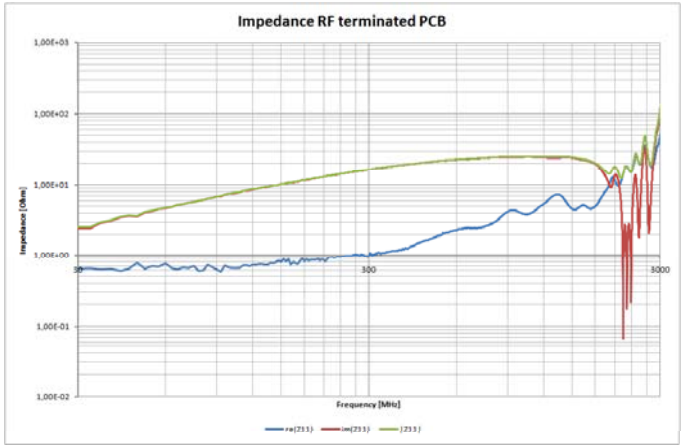
Device port impedance Z_{11}



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Conclusions

- Each part of the PDN chain shall be optimally dampened, by using: series inductance + series resistance or Kelvin contacts
- Decoupling capacitors shall be optimised for ESR too, ESL remains less critical
- Off-chip decoupling, through short PDNs, is too late for decoupling in the sub-ns region (due to self-resonance (skew) and delay of the device's PDN and in its package)
- Resonant-Free PDN is an option.

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