Discrete spread-spectrum sampling (DSSS) to reduce RF emission and beat frequency issues

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***Abstract* — Using spread spectrum clocking techniques with digital systems is quite commonly used to reduce RF emission at the higher harmonics, this to fulfill the existing EMC regulations. Results have been reported frequently. However, with analogue interfaces, fixed frequency sampling is still in place for the sake of signal reconstruction and processing algorithms.**

In this paper the use of discrete spread spectrum sampling is introduced which will not only reduce the RF emission from these analogue-to-digital or digital-to-analog interfaces but will also eliminate the effect of beat frequencies. The beat frequency signal resulting from fixed frequency sampling harmonics and fixed frequency RF interference, will be spread out as sideband noise in the baseband of the intended signal.

A similar DSS technique has been introduced in a patented ABCD power conversion concept using 16 (2^4) fixed frequencies selected randomly.

I. Introduction

In various documents, the RF emission and beat frequency issues of fixed frequency sampling in A/D, D/A converters and class-D amplifiers are elucidated and only partly resolved. On the other hand, with most PCs and full digital applications, spread spectrum clocking techniques are common to blur the RF emission (compared to a defined bandwidth) from the digital part of the system, in particular at the higher harmonics.

When a fundamental clock at 24 MHz is used with 0,5% frequency modulation, a bandwidth of 120 kHz is already occupied. At 24 MHz RF emission is measured with 9 kHz bandwidth, above 30 MHz it is measured in 120 kHz bandwidth. With a frequency modulated distribution being flat, the EMI signal captured in 120 kHz bandwidth decreases with 1/n; n being the odd harmonic number assuming a symmetric system clock.

Due to a fixed sampling interval with A/D and D/A, each time the analogue signal is shortly (Dirac) sampled and then stored; capacitances are charged and discharged causing fixed and steady harmonics. The occurring frequencies are dependent upon the data conversion applied and the signal transfer i.e. storage conditions e.g. when oversampling is used.

To ensure proper digital signal representation, the analogue signal is sampled at a regular interval with minimum jitter, as sampling jitter will cause an error in the sampled analogue signal thus amplitude distortion in the digital represented signal, as the sampling moments are assumed to be equidistant.

II. Overview

With over-sampling, e.g. when an analogue stereo audio signal with a bandwidth of 22,1 kHz is 256 times over-sampled, thus at 5,6 MHz, redundant signal information is acquired. The great advantage of this oversampling method, is that with minimum of aliasing downward (lower side-band) with the original signal will become neglectable even when poor audio low-pass filters are used, e.g. a 1st-order at 1 MHz, at the signal input.

In synchronous clocked A/D, D/A designs and class-D amplifiers, samples are typically taken at the rising edge of the clock. As a compromise, the left and right audio channel can be taken separately at the down and up-going edge of the sampling clock. Typically, the inverted clock signal is used.

With each sampling clock transition, the analogue (audio) signal will be sampled by copying the instantaneous analogue signal's amplitude onto a storage capacitor of a few pF. The few pF signal storage capacitance is taken to assure that during A/D process, charge leakage from that capacitance will be minimal over the A-to-D conversion period: typ. < 1 µs. With each sample taken, the charge necessary to load this storage capacitance to its quantization level has to come out of a signal source or buffer stage in front, which has to have a very low output impedance to allow instant charging. Full charging of the storage capacitance needs to be completed before the conversion process starts.

At each sampling moment charge is instantly drawn from the supply by the buffer's output stage. On-chip decoupling needs to be large compared to the storage capacitances used, to avoid an instantaneous collapse of the internal supply voltage on that buffer stage. After conversion, the charge on the storage capacitance is discharged rapidly before the next analogue signal. sample is taken (or adapted to the new quantization level).

The instantaneous demand of supply current will cause steep off-chip supply currents at a regular time interval, i.e. in the frequency domain a spectrum of clock sample harmonics can be found up into the GHz region as a result of the sub-ns

rise time of the sampling clock(s) to minimize jitter and signal distortion.

With proper on-chip supply decoupling, those higher harmonics resulting in high RF emission can be filtered at the cost of substantial silicon area but the issue of beat frequencies, often being visual or audible, remains unsolved.

With each transition of the sampling clock (rising edges) substantial current is drawn from the supply system. This results in three effects:

- IR-drop due to the average current: ī, which is drawn from the supply system,
- Dynamic supply bounce; îR + L·di/dt;
  î = C·dU/dt
- Intermodulation, due to the non-linearity and the presence of sample clock harmonics and other disturbance source signals which might fold back into the baseband audio or video domain

To sustain an on-chip supply voltage bounce at the analogue buffer stage with a instantaneous supply bounce of 0,5 % or less of the nominal supply voltage, the amount of decoupling capacitance needs to be inversely proportional to the switching i.e. analogue signal storage capacitances (> 200 x larger).

When in a sample clock cycle period e.g. a total capacitance of 4 pF is switched, the decoupling capacitance needs to be > 800 pF assuming no additional IR-losses over the resistive path between the on-chip decoupling capacitance and the signal storage capacitance and the top level supply system will not be capable to deliver instantaneous (re-)charge due to the large RC(L) time constants involved.

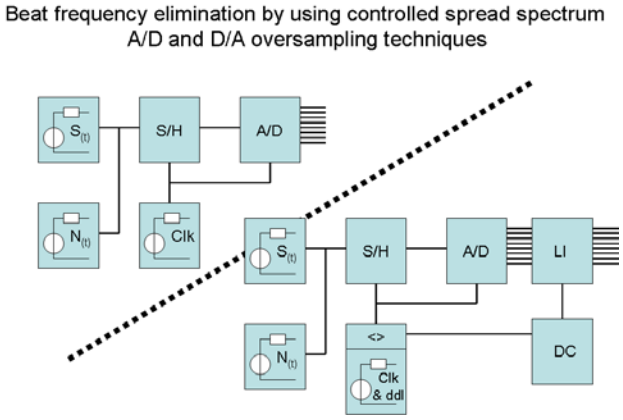

Figure 1 - Bloch diagram of a conventional (upper left) and new approach A/D converter (lower right). S: functional signal, N: (RF) noise, S/H: sample & hold, Clk: fixed (sampling) clock, DDL: digital delay line, LI: Linear interpolator, DC: delay control

Due to the thin supply net structure (typically ≤ 20 % of the TOP metal area) and the inductance of the bond-wires, leadframe and/or laminate/ package interconnect, the on-chip decoupling capacitance will be linearly charged over time (current source charging effect), which results in a sawtooth supply voltage, alike the dynamic supply bounce at the gate/ cell level. When the series inductance is high enough and steady-state power consumption is reached, the dynamic bounce will settle at the nominal supply voltage minus the IR-drop: half the peak-to-peak bounce will be below the on-chip supply voltage and the other half of the saw tooth voltage will appear above that voltage.

A synthesized digital design will yield a gate/cell area fill/utilization of 70 to 85% by automated place and route. With analogue designs, silicon utilization will be better: > 90 %. As a consequence only < 10 % of the silicon area can be filled with gate-oxide decoupling capacitance with an effectiveness of 5 to 20 nF/mm^2. With the above example, several hundred µm^2 of silicon need to be added to the functional design to realize the necessary on-chip decoupling. Compact functional analogue designs appeared small without the necessary decoupling as the required on-chip decoupling can be substantially larger than the analogue circuit itself.

III. New Approach

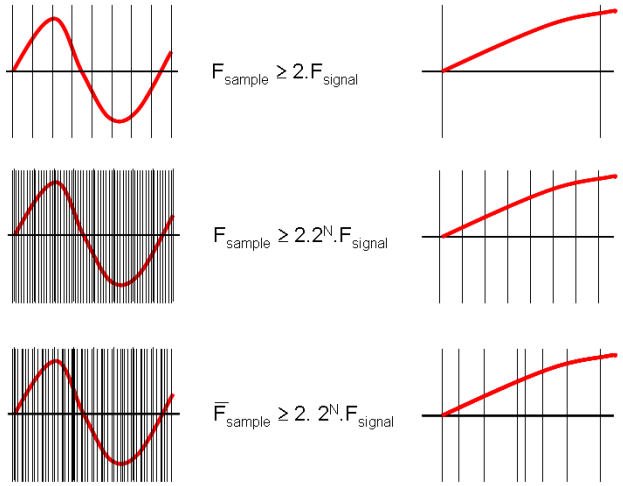

Figure 2 – Equidistant Nyquist sampling a), oversampling b) and DSS sampling c)

With synchronous sampling all activity is periodically. When samples would be taken at predefined but random distributed moments on the 256 times over-sampled clock e.g. using 32 clock samples up and/or downwards, the analogue data can be sampled at other but known sampling moments with an irregular time interval in-between them which may vary between 192 and 320 (256 ± 2 x 32 periods) worst-case and every sample interval in-between. As such, the discrete spread spectrum sample clock varies in frequency between 4,24 and 7,07 MHz, thus 2,83 MHz bandwidth. A block diagram of the conventional A/D design versus the DSSS approach is given in figure 1.

The discrete spread sampling clock is multiplied with the analogue data, figure 1: $S_{(t)}$, which might have had superimposed RF fixed frequency disturbance signals: $N_{(t)}$,

(above the Nyquist frequency) on it, the following advantages are achieved:

- Due to the still synchronous sampling but with a known and pre-defined discrete sample moment modulation, the equidistant sampled signal can be reconstructed after the A/D conversion. When oversampled, a simple linear interpolation algorithm can do this. The same applies for the D/A; when the DSS sampling moment is known on forehand, the linear interpolated digital data pushed forward shall be adjusted to the quantization level as required with the "equidistant" sampling moment.
- Using DSSS, the harmonic RF emission will be distributed over a broad range. The detected disturbance level in a pre-defined bandwidth e.g. 120 kHz at frequencies above 30 MHz will decrease significantly considering the clock spreading proposed. With the audio example given at 5,6 MHz, the 7^{th} harmonic: above 30 MHz, will already span a bandwidth of nearly 20 MHz. As such, the RF emission above 30 MHz is reduced by 44 dB or more. In the FM-band already above 50 dB!
- DSSS for the functional analogue signals will occur as oversampling, DSSS will not have this effect for fixed RF disturbance signals above the Nyquist frequency. After DSSS, followed by linear interpolation, the disturbance signals will be under-sampled and re-occur in the baseband as noise.

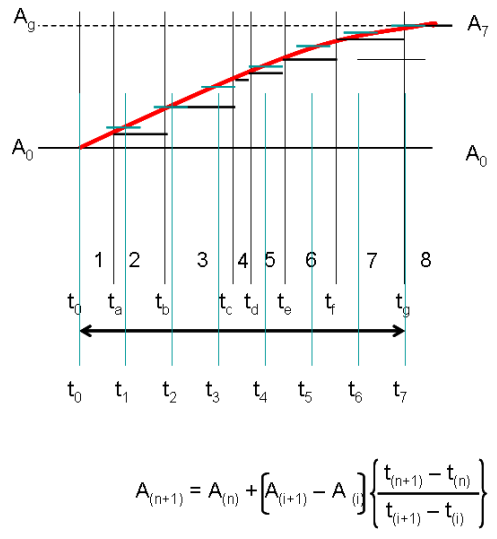

Figure 3 – Equidistant and DSS sampling in detail

In figure 2a, Nyquist sampling is given, where the samples need to be taken at least twice for the maximum occurring functional signal frequency. In case of disturbance signals above the Nyquist frequency, these will fold back as fixed frequency signals into the baseband domain.

In figure 2b, over-sampling is indicated, typically with 2^N increment of samples, the application having similar limitations as the one in figure 2a. In figure 2c, over-sampling with a random distributed sampling rate is given. As long as the moment of sampling is known, the original signal can be reconstructed from the data. For this reason, a low jitter DDL topology has been considered as an implementation solution.

As from the third option, figure 2c and 3, more than necessary data samples to reconstruct the signal are available; the data can be mapped to a linear time scale a processed accordingly, by using the algorithm at the bottom of the figure 3. The linear time scale mapping process is indicated in the figure 3; *t* index *i* is the DSSS sample as where *t* index *N* is the linear time scale data.

At the end of the digital data processing the data stream must be synchronized and mapped to a DSSS format of the D/A or class-D direct signal converter to assure a non-disturbed analogue data representation.

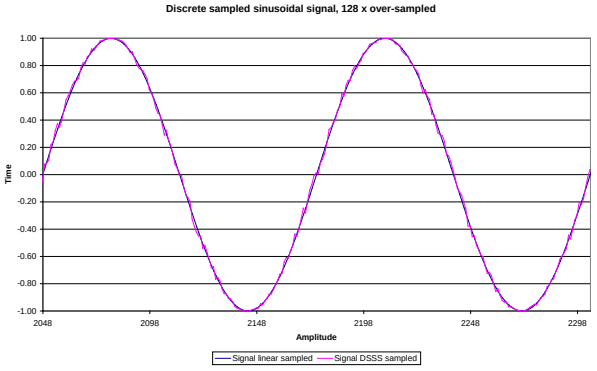

Figure 4 - Linear (blue) and DSS sampled sine wave signal without sample correction (pink)

A frame of a 256 times over-sampled sinusoidal signal sampled and when using DSSS is given in the time domain in figure 4. The DSSS signal shows noisy compared to the equidistant sampled signal due to the wrong allocation of the sample moment, and the addition of a non-correlated RF disturbance signal.

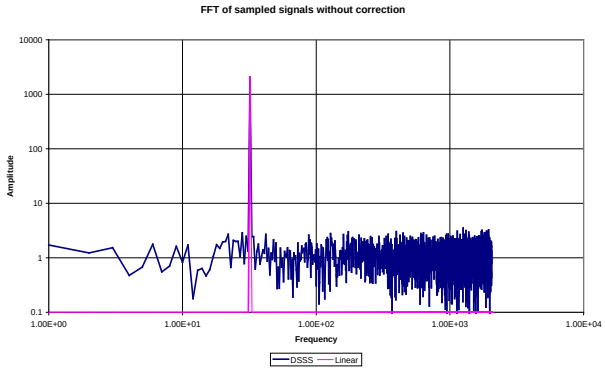

Figure 5 - FFT of an ideal linear sampled sine wave and a non-corrected DSSS signal

From these signals, an FFT is taken, which gives the result in the frequency domain. As the equidistant sampled signal

only gives “zeros” these are set to the base line of the graph, see figure 5.

As can be seen in the frequency domain, the DSSS signal shows noisy compared to the equidistant sampled signal.

After correction of the DSSS samples according to the algorithm, a small delay results from the algorithm but the signal representation shown minor differences with the original, see figure 6.

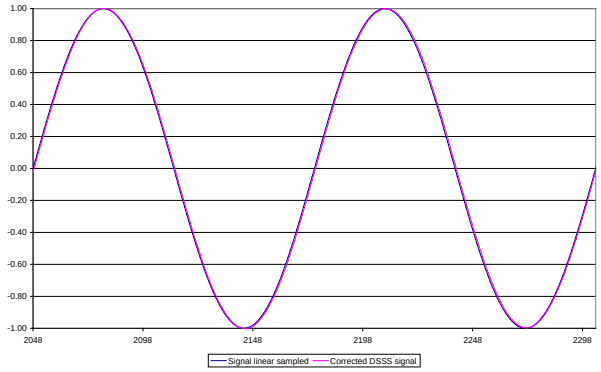

Figure 6 - Original sine wave signal and sine wave after DSSS correction followed by linear interpolation

Following this, also the Fourier transform of the corrected signal is drawn in figure 7.

The higher noise at the lower frequencies is resulting from the artefact that a DC offset remains from the non-correlated RF signal and the rectangular filter window used. By means of a Hamming filter window prior to the FFT analysis, this could have been suppressed and a mirror image of the upper side band noise is expected.

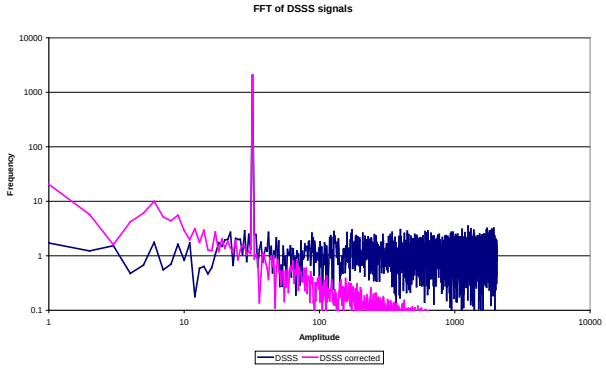

Figure 7 - FFT of a DSS sampled signal, before and after correction

Any fixed and non-fixed frequency RF disturbance signal, above $f_{Nyquist}$, being superimposed on the intended sinusoidal signal will show up as additional symmetrical sideband noise after DSSS data correction rather than a discrete spectral line as a result of the discrete spread spectrum sampling applied.

IV. Conclusions

A simple straightforward discrete spread spectrum (over) sampling approach for analogue signals is given which will substantially reduce RF emission *and* beat frequency issues.

As DSSS clocked signals are no longer symmetric, also even harmonics of the sampling clock will occur.

With the audio example given at 5,6 MHz, the 7th harmonic: above 30 MHz, will already span a bandwidth of nearly 20 MHz. As such, the RF emission above 30 MHz is reduced by 44 dB or more. At higher harmonics, the reduction will be more effective.

The DSS sampling approach can be used with most A/D and D/A applications with limited impact on circuit complexity. With the physical implementation, the DSS sample moments can be obtained from a low jitter voltage controlled digital delay line (DDL) of which the reference i.e. nominal delay is adjusted to a nominal fixed frequency, see figure 1. By delay or pre-count gating or multiplexing the sampling interval can be predefined adjusted. The sampling offsets are set in the digital domain.

In the digital signal domain, the equidistant samples can be obtained by interpolation of the DSS over-sampled data.

The extra digital circuit complexity: DDL and interpolator are minor compared to alternative measures to be taken in the analogue circuitry to achieve similar results. Integration of on-chip decoupling is still recommended (together with accompanying off-chip measures).

No further investigations have been carried out to analyse the effect of higher-order interpolation schemes.

V. References

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